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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/778,915	02/08/2001	Kazuyuki Kikuchi	401071	5831

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EXAMINER	
LIU, ANDREA	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 04/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/778,915	Applicant(s) KIKUCHI, KAZUYUKI	
	Examiner Andrea Liu	Art Unit 2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 February 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 February 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 1-3, 9-11 are rejected under 35 U.S.C. 102(b) as being anticipated by Asai et al. U.S. Patent No. 5,844,263.

The Asai et al. reference shows a method that includes all the limitations recited in the claims . Asai et al. teach a semiconductor integrated device that comprises: a first semiconductor device having a plurality of terminals (col. 1, lines 51-64); and a second semiconductor device having a plurality of terminals, wherein at least some of the terminals of said first semiconductor device are connected with corresponding terminals of said second semiconductor device (col. 1, lines 51 – col. 2 line 5); and a substrate on which said first and second semiconductor devices are mounted, wherein one group of terminals selected from the groups of terminals consisting of (i) the terminals of said first semiconductor device that are connected to corresponding terminals of said second semiconductor device, (ii) the terminals of said second semiconductor device that are connected to corresponding terminals of said second semiconductor device, and (iii) the terminals of said first and second semiconductor devices that are connected to each other, are commonly located (Summary of the Invention, Figure 1).

The Asai et al. reference further teaches the semiconductor integrated device, wherein terminals of said first and second semiconductor device that are connected to each other are arranged opposite each other on said substrate (col. 2, lines 12-40), and that the terminals of the first and second semiconductor devices that are connected to each other, are located on one side of an edge part, and on the second side adjacent to the first side of the said first and second semiconductor devices where the plurality of connecting terminals of said first and second semiconductor device or said second semiconductor devices are located (Summary of the Invention).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 4-8 and 12-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Asai et al. in view of Kanda et al. U.S. Patent No. 6,201,434.

The Asai et al. reference teaches the features outlined above, but it does not explicitly teach the semiconductor device wherein the terminals of the first and second devices that are connected to each other, are arranged in series such that the connecting terminals are related, in order, to each other. The Kanda et al. reference discloses a device wherein such connecting terminals of the group of terminals selected are arranged in series such that these connecting

terminals are related by the prescribed order to each other. In addition, the Asai et al. does not expressly show an oscillating and multiplying unit connected to the power source input terminal and generating a signal with frequency in a semiconductor device with the above stated features.

The use of the step of arranging the connecting terminals in series would have been obvious based on the desired goal of decreasing the wiring region of the substrate. It therefore would have been obvious to one having ordinary skill in the art at the time the invention was made to have advantageously included the step noted above since it is well-known that decreasing the wiring region of the substrate enables the preparation of an inexpensive semiconductor integrated device having a small packaging area. As to the inclusion of the oscillating and multiplying units, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include such units to effectively use the power source of the first device and therefore decrease the number of parts as well as the wiring region of the substrate, allowing for the preparation of an integrated device having a small packaging area.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrea Liu whose telephone number is (571) 272-1901.

Andrea Liu

Patent Examiner

MATTHEW SMITH
SUPERVISORY PATENT EXAMINER
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